Performance Evaluation of Multi-Stages Doherty Power Amplifier for 5G Communication Systems

Shamil H. Hussein, Abdulrahman Kh. Alhafid, Mohammad T. Yaseen, and Ali Dh. Shalal

***Abstract*—This paper presents the design and simulation of a highly efficient three-stage Doherty Power Amplifier (DPA) for 5G wireless communication system at 3.5 GHz using GaAs FET technology. The proposed DPA utilizes optimized dual quarter-wavelength impedance transformers to improve the efficiency and linearity performances of the class AB/C biased main and auxiliary amplifiers. The results obtained show a linear power gain of 7.86 dB with a saturated output power of 35-37 dBm. The maximum PAE achieved at saturation was 74.334% . Around 35% efficiency was maintained at 6 dB output back-off. The proposed amplifier was also tested with a 5G NR modulated signal with an 80 MHz channel bandwidth, and it showed low EVM values of about 1.1–1.3% and ACPR/ACLR better than −36 dBc, indicating good modulation accuracy, spectral confinement, and adjacent-channel suppression. The obtained results confirm the effectiveness of the proposed three-stage DPA in achieving a good trade-off among efficiency, gain and linearity for practical mid-band 5G applications.**

***Index terms*—Doherty power amplifier (DPA), linearity, 5G systems, adjacent channel leakage ratio (ACLR), Error Vector Magnitude (EVM), and output backoff point.**

I. Introduction

Modern wireless communication systems are growing quickly, especially fifth-generation (5G) networks. Because of this, radio-frequency (RF) front-end parts need to be able to work over a wide range of frequencies, be very efficient, and be linear. Power amplifiers (PAs) are now some of the most important and power-hungry parts of wireless transmitters, especially in base station applications [1]. This is because more and more modulation schemes are using less spectrum and having high peak-to-average power ratios (PAPR). Because of this, improving PA efficiency while keeping linear amplification has become a major research goal in the design of modern wireless systems [2]. Conventional linear power amplifiers, such as Class AB amplifiers, suffer from severe efficiency decrease when running at output power back-off (OBO), which is the common operating scenario in 5G systems [3].

Because of its built-in load modulation mechanism, which allows for outstanding efficiency over a broad dynamic range, the Doherty Power Amplifier (DPA) architecture has become one of the best approaches to circumvent this constraint [4-5].

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The DPA is especially suited for contemporary high-PAPR signals because it maintains high efficiency at both saturation and back-off power levels by combining a main (carrier) amplifier with one or more auxiliary (peaking) amplifiers via impedance inverters [6].

Recent research is on the performance improvement of DPA with advanced architecture and semiconductor technologies for 5G applications [7]. The efficiency and linearity performance under high-PAPR signals have been investigated for wideband and asymmetric DPA configurations [8]. Multi-stage DPA topologies have been proposed to improve load modulation and maintain high efficiency over wider output back-off regions. However, many reported designs are still based on complicated matching networks and expensive semiconductor technologies [9]. Thus, efficient and compact multi-stage DPA still remain an important research topic for 5G communication systems.

Multi-stage Doherty architectures get around these problems by using multiple auxiliary amplifiers to improve load modulation and efficiency over a wider range of output power [10]. However, to make these kinds of architectures work in the real world, you need to carefully design the impedance, optimize the bias, and make sure the matching is correct to make sure they are stable, linear, and easy to make. We still need small, efficient multi-stage DPA designs that can get high power-added efficiency (PAE) and good gain using cheap device technologies [11]. Modern 5G systems require highly efficient and linear RF power amplifiers capable of handling high-PAPR signals while maintaining acceptable spectral performance [12]. Wireless technologies are expanding at a very quick pace. A communication system makes it simple to exchange information such as Wi-Max [13] and 5G [14]. The contemporary wireless communications sector is more interested than ever in high-efficiency linear amplifiers that meet modern communications standards. High data rates capable of conveying signals with a high peak-to-average ratio, are offered by modern communications [15].

As a result, the base station amplifiers are typically not operating at their maximum power level, which leads to decreased efficiency. A Doherty amplifier able to meet the prerequisites of a base station power-amplifier in terms of high efficiency is attractive to the wireless industry [16]. To reduce the size of the auxiliary device and at the same time provide the current necessary to modulate the load, a different solution is based on the so-called omnidirectional Doherty arrangement.

This is achieved by balancing the main and auxiliary parts N-1. The paper considered the linearity of the Doherty-

amplifiers in arrangement with a (λ/4) line-impedance transformer in the combined output circuits and with LDMOSFET in the main and peak amplification at 1:1:1 envelope ratio [17]. The main contributions of this work as follows:

- Design and implementation of a three-stage DPA operating at 3.5GHz for 5G applications using GaAs FET technology.
- Development of an optimized output combining network based on dual quarter-wavelength impedance transformers for effective load modulation.
- Comprehensive source-pull and load-pull analysis to maximize PAE and linearity.
- Achievement of high efficiency and linearity, with a peak PAE of 74.3% at saturation and 35% at 6dB back-off.
- Inclusion of ACLR analysis to evaluate spectral performance, demonstrating adjacent channel suppression better than −35 dBc.
- Performance validation through ADS simulations, demonstrating superior efficiency compared to conventional and two-stage DPA architectures.

Despite the extensive research on multi-stage Doherty power amplifiers, limited work has been reported on the implementation of three-stage DPA architectures using GaAs FET technology at mid-band 5G frequencies. In this work, a systematic design approach is presented based on source-pull and load-pull optimization combined with a dual quarter-wavelength impedance transformer network. In addition, a fair comparative analysis between single-stage, two-stage, and three-stage DPA configurations under identical operating conditions is conducted to highlight the performance improvement in efficiency and linearity. These aspects distinguish the proposed work from previously reported.

This article is organized as follows. Section I introduces the background and motivation of the study and highlights the main contributions. Section II describes the operating principles and circuit design of the Doherty power amplifier. Section III presents the design methodology of the proposed three-stage Doherty power amplifier. Section IV discusses the simulation results and performance analysis. Finally, Section V concludes the paper and outlines of the work.

II. Related Works

Recent wireless communication systems, particularly 5G networks, require RF power amplifiers with high efficiency and linearity for high peak-to-average power ratio (PAPR) signals. The conventional Class AB amplifiers suffer from efficiency degradation at the output back-off regions. The Doherty Power Amplifier (DPA) architectures are an attractive solution due to their load modulation capability and improved back-off efficiency [18–19].

Several research have focused on enhancing two-stage DPA through impedance matching approaches, harmonic tuning, and bias optimization. For example, Nasri et al. [20] demonstrated a wideband GaN-HEMT-based DPA working at 2.8GHz and 3.6GHz for 5G applications. The proposed circuit was operated at frequencies of 2.8GHz and 3.6GHz. The configuration of DPA is class AB/C for main and Aux amplifiers respectively. The simulation results obtained were a good trade-off between linearity and efficiency. It provided output power of about 43dBm at saturated. In addition, the power gain is 8dB. The drain efficiency was 60% and 43% at both saturated and output power back off regions respectively.

Ken, Darwish, and Zaghloul presented a compact Doherty power amplifier (DPA) circuit in 2019 by [21] for broadband communication systems applications. The proposed DPA is operated at a frequency of range from 1.7GHz to 3.4GHz. The simulated saturated output power was about 40dBm by using GaN HEMT device technology. The peak value of the power added efficiency was obtained about 60% and 37% at the saturated and output power backoff (OPBO) respectively.

The three-stage asymmetric Doherty power amplifier (ADPA) was introduced by Son, Kim, and Lee in 2011 [22]. Using GaN HEMT devices operating at 2.6 GHz for WiMAX signals with a bandwidth of 5MHz and an average power ratio of 8.3 dB, the suggested APDA has been put into practice. The simulation results showed that the output power and power added efficiency are 51.7 dBm and 60.4% at the saturated point of the amplifier. The ADPA meets the linearity requirement with a neigh-boring channel leakage ratio of -51.98dBc at 10MHz offset after linearization utilizing the digital feedback predistortion approach.

Zhou et al. [23] introduced a three-port harmonic injection network to extend the efficiency range of a DPA, while Zhu et al. [24] proposed a modified load modulation network to achieve high relative bandwidth and efficiency.

Three-stage and multi-way Doherty power amplifiers are getting more and more attention because they might be able to keep high efficiency over a wider dynamic range. Li et al. [25] created a three-stage high-power DPA using GaN-HEMT technology. This showed better load modulation and higher efficiency. Some other research has looked at Doherty architectures that use broadband and filtering to find the right balance between efficiency, gain, and bandwidth [26]. Even with these improvements, many reported designs still use complicated output combining networks or advanced semiconductor technologies, which could make the design process more difficult and expensive [27].

Recent DPA research has shown that GaN-HEMT and CMOS technologies are the most popular. But GaAs FET-based designs are still interesting because they have good gain characteristics, are well-developed, and work well with mid-band 5G frequencies. But not many studies have looked at three-stage Doherty architectures that use GaAs FET technology and a systematic approach to optimizing source-pull and load-pull at 3.5 GHz. There also aren't many full comparisons of single-stage, two-stage, and three-stage Doherty setups that use the same conditions.

This study focuses on the design and simulation of a three-stage Doherty power amplifier using GaAs FET technology for 5G applications at 3.5 GHz, which is different from what has been done before. The proposed design achieves improved power-added efficiency and linearity across saturation and output back-off regions by using an optimized dual quarter-wavelength impedance transformer network and load-pull based matching. This makes it a competitive and practical solution for 5G base-station transmitters.

III. Doherty Power Amplifier Circuit Design

In wireless base stations, the RF power amplifier (PA) dominates the overall power consumption. Therefore, there is a great need to improve the efficiency of a PA [28]. The Doherty power amplifier (DPA) uses two transistors to perform load modulation at the fundamental (fo) frequency, keeping a high efficiency from a certain output power back-off (OBO) level up to full-power [23]. The two transistors that are already present in the DPA can be used to perform the active harmonic injection; the harmonic component generated by one transistor can be injected into the drain.

To maximize PA performance, the Doherty amplifier employs two amplifiers. The peaking amplifier, also known as the auxiliary amplifier, manages the high-power zone, while the carrier amplifier, also known as the main amplifier, handles the low-power sector. Although it sounds easy, there can be difficulties in putting this into practice [29]. A traditional Doherty amplifier is seen in Fig. 1 with two amplifier paths that are each supplied by a hybrid coupler. Until the signal enters the high-power area, the peaking amplifier is inactive and the carrier amplifier is constantly on. The peaking amp activates and offers amplification in the high-power range to meet the increased output power. One of the two major design problems is to separate and reassemble the signal while keeping time alignment. The second is enabling peaking amplifier while preserving linearity [30].

It is crucial that the carrier and peaking amplifiers operate linearly together as many modulation techniques rely on preserving amplitude and phase purity. The carrier amplifier is referred to as working in Class A, Class B, or Class AB in various articles; the essential idea is that the amplifier must function linearly.

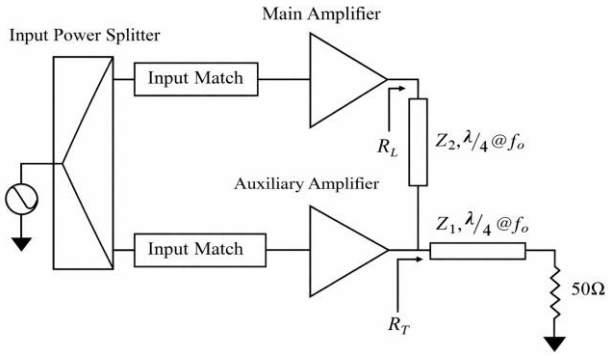

Fig. 1. Schematic diagram of the Doherty power amplifier [30].

It is common to refer to the peaking amplifier as functioning in Class C, which denotes that it is biased just partially. Class C amplifiers may not be appropriate for amplifying all modulation types since they are typically associated with non-linear operation. To retain linearity at the output, the Doherty amplifier, on the other hand, integrates the peaking amplifier as an add-on component. Using a quarter-wave (λ/4) transmission line, the traditional Doherty design produces an impedance inversion at the carrier amplifier's output. To align the two routes, a second quarter-wave line is added ahead of the peaking amplifier because the first one causes a 90° phase shift. To match the impedance to 50 Ω, there is typically an extra quarter-wave line at the Doherty amplifier's output. Transmission lines are replaced in certain designs by lumped circuit parts [31].

In order to sustain efficiency in the back-off area beyond the limitations of the traditional design, the multi-way Doherty amplifier concept is employed. In order to maintain the output power relations between the peaking and carrier cells, the amplifier cells' output impedances must be chosen. It should highlight, therefore, that transmission lines with characteristic impedances that are either too high or too low in the output combining circuit are not feasible to implement. As seen in Fig. 2, a three-way Doherty circuit is made up of three amplifiers: the "main" and the "Aux-1, Aux-2. It was discovered that the output combining network's quarter-wave transformers' characteristic impedances were R_1=50Ω and R_2=16.7Ω, whilst the characteristic line-impedance, Rt = 25Ω [25].

The impedance, the bias, and the matching network are all important parts of the suggested Doherty power amplifier. The load-pull and source-pull tests have been used to find the best source and load impedances. This is done to get the most work and power out of it. Setting the bias settings for the peaking and carrier amplifiers correctly is very important. This will make sure that the output back-off works smoothly and the load modulation is correct. Quarter-wavelength transmission lines are also used to make the matching networks, which are carefully tuned to work well at all frequencies and change impedance correctly. The proposed DPA will work better if you do all of these things at once.

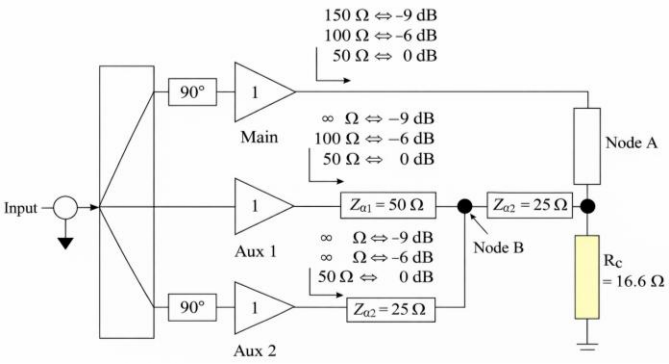

Fig. 2. Block Diagram of Three-Stage Doherty power amplifier [25].

IV. Design of Three-way Doherty Power Amplifier

In order to design the Doherty power amplifier (DPA) circuit, there are several steps required including, Selection of transistors with DC analysis must be performed using the Load line theory. Secondly, source pull and Load-pull technique need to be performed for input and out matching network circuit design. The Third step is Impedance matching, followed by Circuit simulation. Finally, the results are performed. The low and high voltage power supply of the transistor for the proposed power amplifier like -2V for gate-source voltage (V_{GS}), and 3V for drain-source voltage (V_{DS}) [32]. All of the voltage levels, impedance values, and performance metrics are written out in the same way throughout the manuscript to make everything plain and consistent. OBO stands for "output back-off," and all

impedance values are stated in ohms. This makes it easy to read and makes sure that the analysis is always the same. When designing something, load/source-pull analysis is performed to discover the best impedance, the proper bias tuning (class AB/C), and matching networks that use quarter-wave transformers. This makes sure that load modulation works well and that the impedance is set up correctly.

By varying the load-impedance that the device-under-test (D-U-T) perceives, the load pull approach allows for the simultaneous measurement of the DUT's performance. The DUT's performance for different source impedances is also quantified in source pull. The measured results are very helpful in figuring out what the device needs to see as its ideal load and source impedance in order to operate at peak efficiency. In instance, load pull is frequently used to calculate the load impedance needed to maximize efficiency. A power amplifier typically requires a source pull, but it is not always necessary. Instead, the input is conjugate matched. Note that there is bias in the calculated impedance values [32].

Load pull and source pull were used in this work to achieve the highest possible PAE. The outcomes of these simulations demonstrate that, at frequency of 3.5GHz, the source and load impedances are (1.433+j*2.57)Ω and (8.835+j*4.05)Ω as depicted in Figs. 3 and 4. The input transmission line λ/4, input source impedance, and input matching network are all equivalent to 50Ω. Power supply V_{low} of -2V for the carrier amplifier's biasing, $V_{low1,2}$ is -2.6V for the peaking amplifiers' biasing, and V_{high} voltage for carrier and peaking amplifiers.

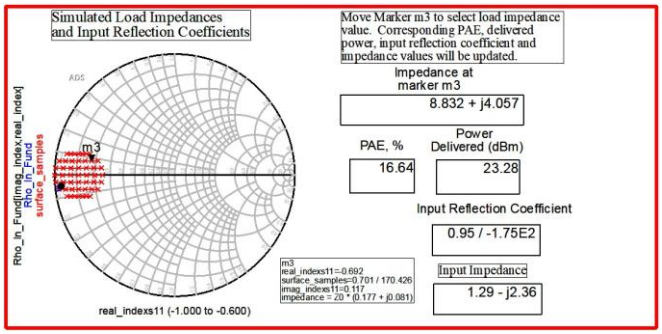

Fig. 3. Load-pull analysis for achieving maximum efficiency.

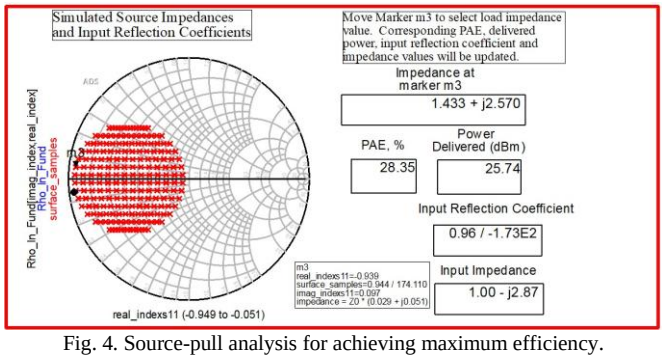

Fig. 4. Source-pull analysis for achieving maximum efficiency.

V. Simulation Results and Discussion

The three-stage DPA amplifiers were analyzed and designed using the ADS library package for broadband communication applications such as 5G systems. The active GaAsFET devices used in the main and auxiliary amplifiers of the DPA are biased in class AB and C, respectively. A one-tone simulation was performed at the frequency of 3.5 GHz. The design of multi-stage DPA amplifiers involves a number of steps, including input and output matching networks, DC analysis, bias voltage, source-pull and load-pull characterization. Fig. 5 Simulated PAE performance of the proposed three-stage DPA at 3.5 GHz. The amplifier obtained the maximum PAE of 74.334% in the saturated output power from 35 dBm to 37 dBm, showing high efficiency performance for 5G applications. Fig. 6 shows the full schematic implementation of the proposed three-stage DPAs based on one-tone simulation analysis using ADS software.

It's important to remember that the results shown here come from a study that only looked at one tone. This is a common way to test the linearity, gain, and efficiency of RF power amplifiers. This study looks at both important performance metrics like power-added efficiency (PAE), AM-AM, and AM-PM characteristics, as well as more advanced modulation performance requirements like the Adjacent Channel Power Ratio (ACPR). The ACPR is an important number for figuring out how much interference there is between adjacent channels in modern communication systems like WCDMA and OFDMA. This is especially true when modulation becomes more complex. To find the value, divide the average power in the primary channel by the average power in the channel next to it. The results show that the recommended amplifier has an ACPR of more than -40 dBc when it is running at its highest output power of about 40 dBm. This means that it is very linear and that channels that are close to it don't bother it too much.

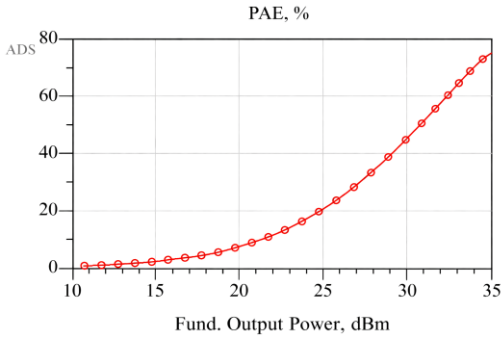

Fig. 5. The power added efficiency of DPA at the frequency of 3.5GHz.

The performance of the three-stage Doherty Power Amplifier's is studied in detail in Figures 7-9, evidencing high linearity, matching efficiency, and dynamic range. The superior linearity behavior of the DPA is demonstrated in Fig. 7, revealing 1 dB/dB and 0.18°/dB AM-AM and AM-PM, respectively, at 20 dBm input power, and therefore minimal signal and phase distortions that are essential for the preservation of the modulation accuracy in 5G systems. The obtained AM-AM and AM-PM results indicate low amplitude and phase distortion, which are essential indicators of linear amplification performance. These characteristics provide an initial assessment of signal integrity and suggest that the proposed DPA is suitable for handling high peak-to-average power ratio (PAPR) signals in 5G systems.

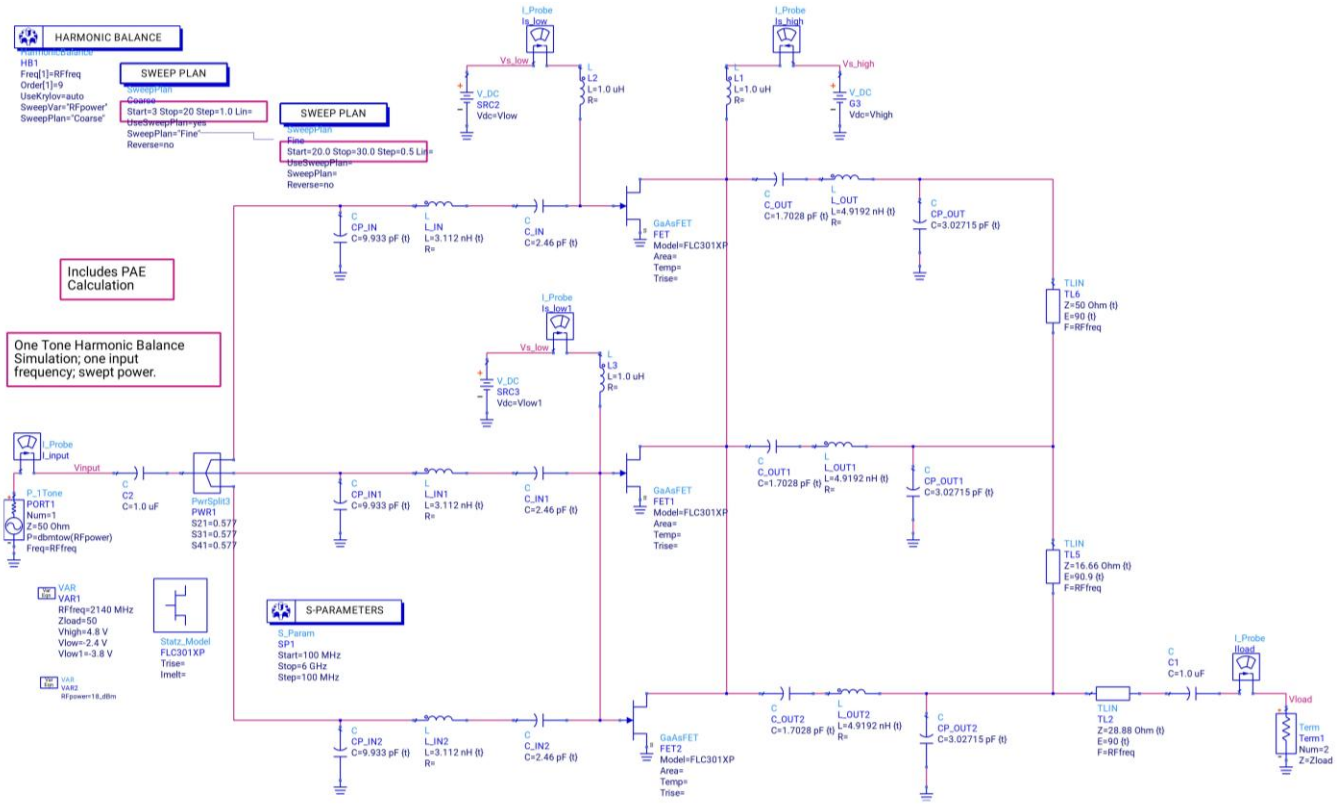

Fig. 6. Full schematic circuit of the three-stage Doherty power amplifier.

The Adjacent Channel Leakage Ratio (ACLR) is a way to see how well modulated signals work in a straight line. This is important for 5G systems. Fig. 8 shows the simulated output spectrum of the proposed three-stage DPA using a 5G NR signal with 80 MHz bandwidth at 3.5 GHz. The proposed amplifier achieved an ACPR of approximately -36 dBc, indicating good adjacent-channel suppression and acceptable linearity performance for 5G applications.

These results indicate improved linearity performance and effective suppression of adjacent-channel spectral components. The parts of the adjacent channel are effectively blocked below the main signal band. This shows that the suggested design meets the ACLR performance standards that are good enough for 5G applications. This result is in line with the AM-AM and AM-PM characteristics, which means that the proposed amplifier can handle signals with high PAPR.

The simulated EVM and ACPR characteristics of the proposed three-stage DPA versus output power are shown in Fig. 9. The EVM is maintained in a low range of about 1.1-1.3 % over the region of useful output power with good in-band modulation accuracy and limited amplitude/phase distortion. In the meantime, the ACPR is enhanced to about −36 dBc at higher output power levels, which verifies the effective suppression of adjacent-channel spectral regrowth. The results demonstrate that the proposed DPA offers a good trade-off between modulation accuracy and spectral linearity, which supports its suitability for 5G NR applications.

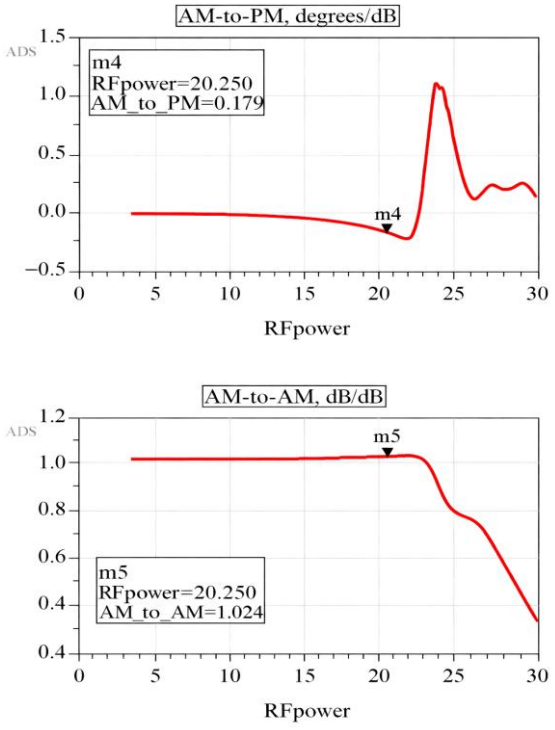

Fig. 7. The simulated of both amplitude distortion and phase distortion for DPAs.

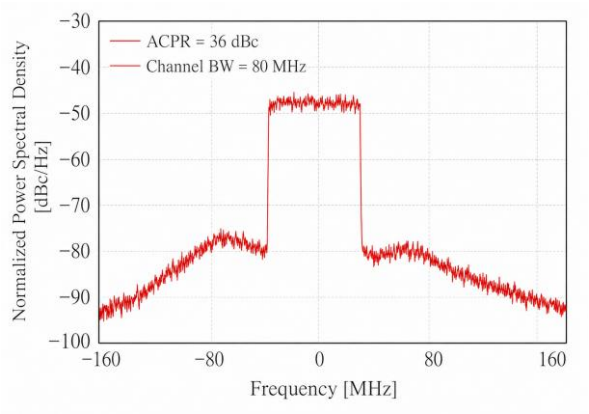

Fig. 8. The simulated output spectrum of the proposed DPAs based on 5G channel bandwidth 80MHz signal at the frequency of 3.5GHz.

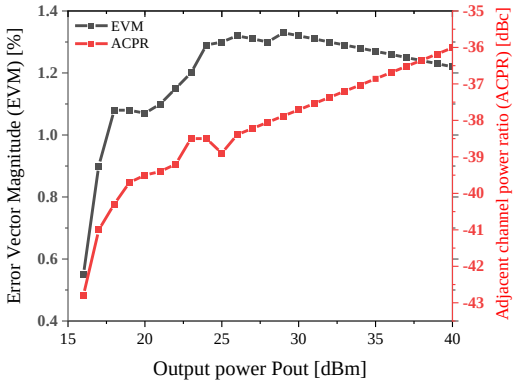

Fig. 9. The simulated EVM and ACPR of the proposed DPAs as a function of the output power for 5G modulated signal using 16 QAM

Fig. 10 shows the simulated effective input and output matching performance of the proposed three-stage DPA. The reflection coefficients (S_{11}/S_{22}) are well impedance matched at 3.5 GHz for efficient power transfer and stable operation. Fig. 11 also illustrates the dynamic behavior of the amplifier. The output power rises nearly linearly with the input power until the saturation region of about 35 dBm. The obtained results confirm the feasibility of the proposed three-stage Doherty architecture with high efficiency over a wide operating range due to the load modulation mechanism. Moreover, the amplifier achieves a peak PAE of 74.334% at saturation with acceptable linearity characteristics. The transducer gain is about 7.9 dB before a gradual gain compression is observed near saturation. The measured P_{1dB} is observed at about 29 dBm input power. The results suggest that the proposed DPA offers a good compromise between efficiency, gain, impedance matching, and linearity and is appropriate for 5G base-station applications dealing with high-PAPR signals.

The transducer power gain is seen to peak at 7.8 dB when the output power is 30 dBm, right before the device is saturated, in Fig. 12, which further illustrates this relationship. According to these results, the DPA can achieve high efficiency and big gain over a wide range of AM-AM, which could be useful for 5G applications that require both linearity and power efficiency. The impact on system performance of the trade-off between PAE optimization and gain compression, which can be accomplished using a three-stage Doherty structure for high PAPR signals, is emphasized.

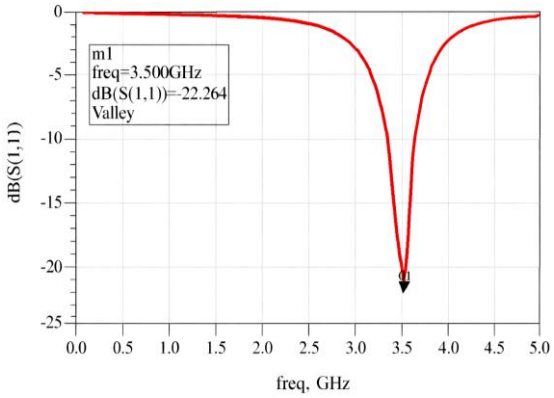

Fig. 10. The simulated reflection coefficients (S11) of 3-stages DPAs at the operating frequency.

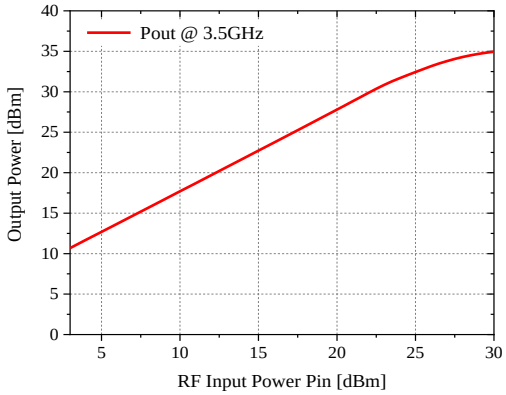

Fig. 11. The simulated output power of DPAs as a function of RF input power.

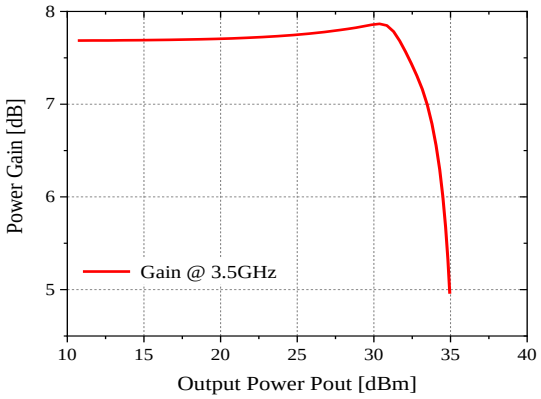

Fig. 12. The simulated transducer power gain against of power saturated output.

In order to evaluate the linearity of the DPA circuit design is the output spectrum harmonic. It represents the figure of merit which is measured by dBc. Fig. 13 showed these order harmonics as a function of the input RF power. It can be observed that the 3rd harmonic was rising with increasing RF power input. However, it is reduced by -20dBc with a range from -60dBc to -80dBc at the RF input power of about

25dBm. Therefore, the overall difference of 1st and 3rd harmonic is about -40dBc. So, the proposed DPA gives a good output spectrum performance.

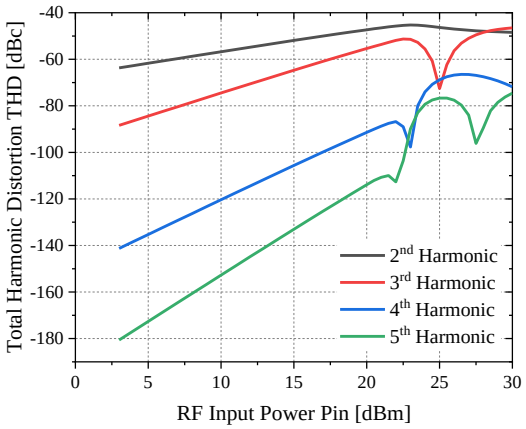

Fig. 13. The simulated output spectrum THD of the proposed DPAs at different RF input power.

The single, two, and three stages DPA circuits have been simulated and performed using ADS software at the frequency of 3.5GHz. The simulated results showed that the proposed three-stage DPA has a high power-gain, the PAE%, and power out at the saturated and output-backoff regions compared to others. Fig. 14 shows the power added efficiency PAE% of the proposed DPA amplifier circuits as a function of the output power at the saturated region. It is clear that the proposed DPA with three stages has a high PAE compared to conventional PAs which are considered 75%.

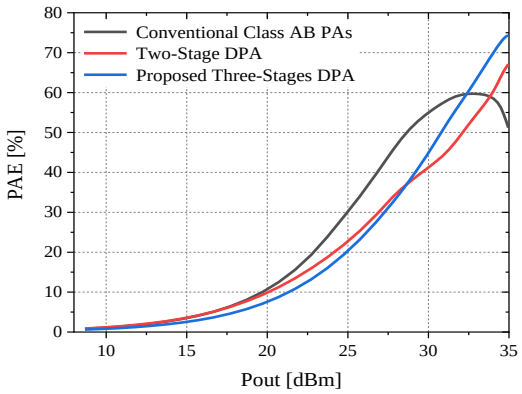

Fig. 14. The simulated PAE% of the proposed 3-stages DPA compared to traditional PAs as a function of output power.

The proposed three-stages DPA circuit has a high linearity and drain efficiency compared to class AB and conventional DPA amplifiers at the output power back-off points (OBO) (-6dB) as depicted in Fig. 15. It is observed that the PAE% are about 35%, 29%, and 16% at -6dB OBO region for 3-stage, 2-stage, and conventional PAs respectively.

The performance of the three-stages proposed DPA were summarized and compared to other studies in Table 1. The proposed DPA was designed with the same device and was intended to target an output OBO level that was similar across the same frequency range. In addition, the main goal was achieved in this work is high power added efficiency with suitable power gain at the resonant frequency. Finally, the proposed DPA can be a candidate for 5G applications. It is important to note that the results shown are based on simulation analysis using ADS with realistic device models.

The results show that the proposed design has good efficiency and linearity, but more testing is needed to see if it can be used in real life. In the future, the focus will be on making the hardware and testing it in real-world conditions. It is important to note that the analysis presented here is mostly about the center frequency of 3.5 GHz, which is an important mid-band frequency for 5G applications. The proposed design shows stable performance at this frequency, but a full analysis of broadband frequencies is not possible in this study. The proposed amplifier's performance over a wider frequency range will be tested in future work to confirm its ability to work with a wide range of frequencies.

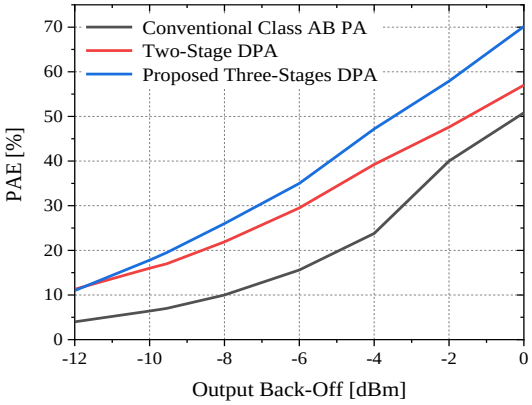

Fig. 15. The simulated Output back-off power added efficiency of DPA amplifier compared to conventional power amplifier.

TABLE I
PERFORMANCE COMPARISON OF LITERATURE REVIEW WITH RESPECT PROPOSED DPA

Ref. Year	Freq. [GHz]	Technology Transistor Device	Pout [dBm]	PAE Sat. [%]	PAE OBO [%]	Gain [dB]
[17] 2021	2.45	GaAs FET	32	61.8	35	8
[20] 2021	3.6	GaN-HEMT	43	62	44	8
[21] 2019	3.4	GaN-HEMT	40	60	37	8
[33] 2023	3.5	0.5µm GaAs HBT	27.8	34.3	25	7.8
[34] 2024	2.6	0.18µm CMOS	21.3	35	23	≤ 10
[35] 2025	3.3-4.2	GaAs HBT	34.8	43	28	9
[36] 2025	5-7	GaAs HBT	26.5	32	27.8	13
[37] 2024	3.3-4.2	2µm GaAs HBT	34.8	43	31-34	≥ 10
This work	3.5	0.5µm GaAs FET	38	75	36	8

The proposed three-stage GaAs FET DPA achieved ACPR/ACLR better than -36 dBc with low EVM values of about 1.1-1.3% using an 80 MHz 5G NR modulated signal at

3.5 GHz, indicating good spectral confinement, modulation accuracy and linearity performance for practical 5G applications. Table 1 is a comparison, which is to be a broad overview of performance because of the differences in technologies and operating conditions. Nevertheless, the proposed design still shows competitive efficiency and linearity characteristics.

VI. Conclusions

This paper presents the design and simulation of a high efficiency 3-Stage Doherty Power Amplifier (DPA) for 5G applications at 3.5 GHz using GaAs FET technology. The proposed DPA achieved a peak PAE of 74.334% at saturation with the output power in the range of 35-37 dBm and about 35% efficiency at 6 dB output back-off. The efficiency at the back-off region was enhanced in comparison with the conventional Class AB and two-stage DPA architectures. The amplifier also exhibited good linearity performance with power gain of 7.86 dB, low AM-AM and AM-PM distortion, and proper impedance matching with reflection coefficients less than −40 dB. The proposed design was further validated with a modulated 5G NR signal having a bandwidth of 80 MHz. The measured EVM was 1.1–1.3% and the ACPR/ACLR was better than −36 dBc, confirming good modulation accuracy and adjacent-channel suppression under high PAPR conditions. The results of the ADS simulation show that the proposed three-stage DPA offers a good compromise between efficiency, gain and linearity, making it a promising candidate for practical mid-band 5G base-station applications. Future work will be focused on the fabrication and experimental validation of the proposed three-stage Doherty power amplifier in a hardware prototype. Practical measurements will be carried out for output power, PAE, ACLR, EVM, gain and thermal performance with real 5G NR excitation signals to validate the simulation results. Moreover, broadband operation and digital predistortion (DPD) techniques will be investigated to further enhance the linearity and efficiency performance of the proposed architecture in practical base-station environments.

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