A Novel Approach to Design 2-bit Binary Arithmetic Logic Unit (ALU) Circuit Using Optimized 8:1 Multiplexer with Reversible logic

Vandana Shukla, O. P. Singh, G. R. Mishra, and R. K. Tiwari

***Abstract*— Reversible circuit designing is the area where researchers are focussing more and more for the generation of low loss digital system designs. Researchers are using the concept of Reversible Logic in many areas such as Nanotechnology, low loss computing, optical computing, low power CMOS design etc. Here we have proposed a novel design approach for a 2-bit binary Arithmetic Logic Unit (ALU) using optimized 8:1 multiplexer circuit with reversible logic concept [1]. This ALU circuit can perform complement, transfer, addition, subtraction, multiplication, OR, XOR, NAND functions on given values. The ALU circuit has been simulated on Modelsim tool and synthesised for Xilinx Spartan 3E with Device XC3S500E with 200 MHz frequency. This 2-bit ALU using reversible logic is useful for the designs of low power loss systems.**

Keywords*— *Reversible circuit design, 2's Complement, Comparator, Adder, Subtractor, Multiplier, Reversible gates, Multiplexer circuit

I. INTRODUCTION

Arithmetic Logic Unit (ALU) is a vital component of any computing system. It is a digital circuit that performs the required arithmetic as well as logical operations on the operands. Earlier Von Neumann proposed first ALU in 1945 when he was working on EDVAC [2]. Conventionally ALUs were designed using basic logic gates such as AND, OR, NOT etc. However these gates dissipate some amount of energy due to the information loss during the operation. The amount of energy loss for one bit of information loss was calculated as kTln2 joules by R. Landauer in 1961 [3]. In 1965 G. E. Moore has given his famous Moore's law in which he stated that the number of transistors incorporated on a unit chip area doubles in an approximate time span of two years [4]. As a result of increase in the component density the amount of heat loss increases exponentially. In 1973 C. H. Bennette has shown that this amount of heat generation or energy loss can be minimized or removed (ideally) from the system by redesigning the same digital circuit using reversible logic gates [5].

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Earlier Lekshmi Viswanath et al proposed a reversible ALU circuit in 2012 which perform three arithmetic and five logical operations [6]. After that, in the same year Akansha Dixit et al proposed a new approach to design ALU circuit using reversible logic which perform increment, decrement, addition, subtraction, OR, XOR, AND, transfer and complement operations [7]. Later in 2014 S. Anusha et al has given a novel approach to design the ALU circuit with reversible logic using Arithmetic, logic, shift and multiplier circuit block [8].

This paper is organized in six sections to provide the clear view of the proposed ALU circuit. Section I and II provide the introduction of the research work and fundamental concepts of reversible logic concept respectively. After that section III and IV provide the knowledge about the concept of 2-bit ALU circuit and proposed approach to design 2-bit ALU using reversible logic respectively. Result and analysis of the proposed design approach is provided in the section V and conclusion of the paper with future scope is elaborated in the section VI at the end.

II. REVERSIBLE LOGIC FUNDAMENTALS

The fundamental concepts of Reversible logic are described in following subsections in brief:

A. REVERSIBLE LOGIC GATES

Reversible logic gates are described as (n, n) digital gates where n, n represents equality of number of input and output signals [9-11]. Any reversible logic gate must have following features:

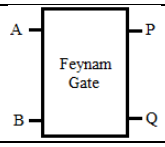
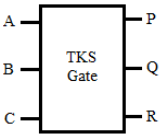
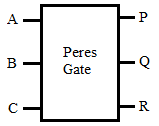
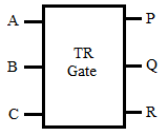
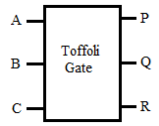
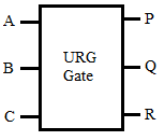
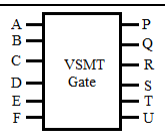
[1] Equal number of bits in input and output.
[2] One to one mapping between input and output bits.
[3] Fan-out of each gate must be equal to one.

In reversible logic gates, we can generate the applied input combination by knowing the output status at any instance. Above features discriminate these gates from the existing conventional (irreversible) logic gates.

B. EXAMPLES OF REVERSIBLE LOGIC GATES

Researchers have proposed various reversible logic gates. Some of which are illustrated in table 1 in the form of block diagram, size and output equations etc.

TABLE I
EXAMPLES OF SOME REVERSIBLE LOGIC GATES

S. No.	Name of Reversible Logic Gate	Size of the Gate	Block Diagram	Output Equations
1	Feynman Gate [12]	2×2		P = A; Q = A⊕B;
2	TKS Gate [13]	3×3		P = A.C' + B.C; Q = A⊕B⊕C; R = A.C + B.C';
3	Peres Gate [14]	3×3		P = A; Q = A⊕B; R = A.B⊕C;
4	TR Gate [15]	3×3		P = A; Q = A⊕B; R = A.B'⊕C;
5	Toffoli Gate [16]	3×3		P = A; Q = B; R = A.B⊕C;
6	URG Gate [10]	3×3		P = (A+B) ⊕C; Q = B; R = A.B⊕C;
7	VSMT Gate [17]	6×6		P = E'.(A.F'+B.F)+ E.(C.F'+D.F); Q = A⊕B⊕C; R = E⊕F; S = C⊕D; T = D⊕E⊕F; U = E;

C. CONSTANT INPUT SIGNALS

These are additional signals required at the input stages of reversible logic gates to complete the designed circuit using reversible logic approach. These constant input signals may be either high or low according to the requirement of the desired working of the designed circuit.

D. GARBAGE OUTPUT SIGNALS

These signals are defined as those unwanted additional signals generated from the designed reversible circuit to complete the working of the circuit according to the requirement of the target system. These signals are equivalent to the bit loss in the irreversible gates as garbage signals are unused output signals.

E. QUANTUM COST

Quantum cost of any reversible logic gate or circuit is defined as the required number of 1×1 or 2×2 basic reversible gates to design the same. The quantum cost of 1×1 reversible gate is zero and that of 2×2 reversible gate is 1. So the overall cost of reversible gate or circuit can be calculated based on the required number of these basic reversible gates.

F. REVERSIBLE CIRCUIT DESIGN

This concept aims to replace the design entities of the target digital circuit with reversible logic gates to design the same with reversible approach [18-21]. The designed reversible circuit must have following features:

[1] Use of minimum number of reversible gates to design the target circuit.

[2] Generation of minimum (ideally null) number of garbage output signals from the designed reversible circuit.

[3] Requirement of minimum (ideally zero) number of constant input signals.

[4] Minimum total quantum cost of the circuit.

[5] No feedback connection in the designed reversible circuit.

III. TWO-BIT ARITHMETIC LOGIC UNIT FUNDAMENTALS

Arithmetic logic unit is a vital component of any computing system. It performs all the necessary arithmetical as well as logical operations on the data to provide the required output. Here we are planning to design a small ALU circuit which performs some arithmetical as well as some logical operations on the two bit binary operand. Following components are required to design this proposed ALU circuit:

A. Complement Circuit

This circuit provides the 2's complement of the entered two bit binary input number. Figure 1 shows the complement circuit using conventional basic logic gates and corresponding block diagram of the complement circuit.

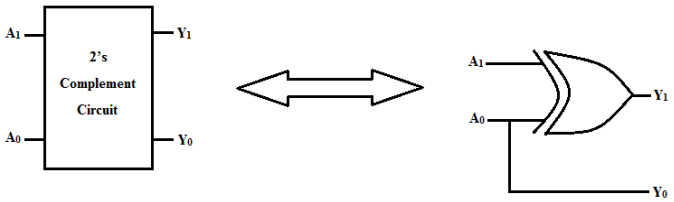


Fig 1: Block diagram and logic implementation of Complement Circuit using conventional approach

Here output equations are as follows:

$Y_1 = A_1 \oplus A_0$;

$Y_0 = A_0$;

B. Transfer Circuit

This circuit transfers the applied signals to the output side after some time delay only. Figure 2 below shows the block diagram as well as conventional circuit of transfer circuit of proposed ALU for 2-bit binary numbers.

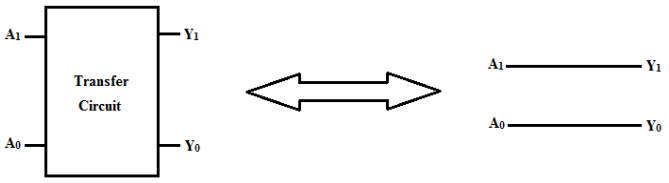


Fig 2: Block diagram and logic implementation of Transfer Circuit using conventional approach

Where $Y_1 = A_1$ and $Y_0 = A_0$ respectively.

C. Adder Circuit

This circuit adds the applied bits of the binary number and provide the sum and carry bits of the result. Figure 3 below shows the block diagram and conventional digital circuit for this adder part of the proposed ALU circuit.

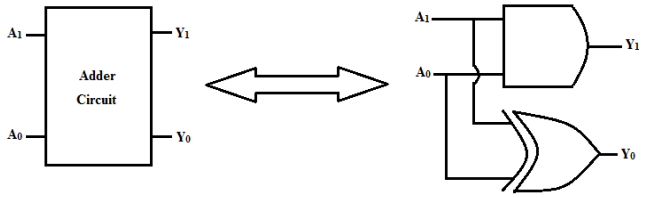


Fig 3: Block diagram and logic implementation of Adder Circuit using conventional approach

Where output bits are illustrated as follows:
Y_1 = Carry = $A_1.A_0$;

Y_0 = Sum = $A_1 \oplus A_0$;

D. Subtractor Circuit

This circuit subtracts the LSB (A_0) from MSB (A_1) of the applied binary number to provide the difference between the applied bits. The design of subtractor circuit using conventional approach is illustrated in figure 4.

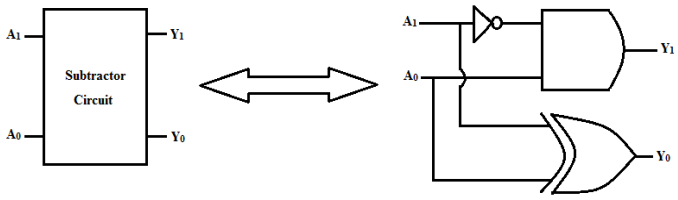


Fig 4: Block diagram and logic implementation of Subtractor Circuit using conventional approach

Where output bits are calculated as follows:
Y_1 = Borrow = $A_1'.A_0$;

Y_0 = Sum = $A_1 \oplus A_0$;

E. Multiplier Circuit

This part of the ALU multiplies the applied bits of the binary number and provide the required multiplication result. We have shown the block diagram and design of this multiplier circuit using conventional irreversible gates in figure 5.

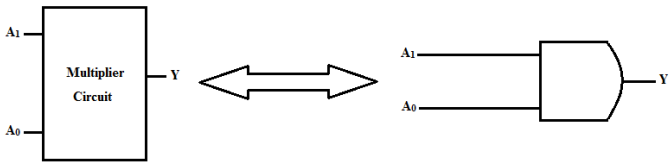


Fig 5: Block diagram and logic implementation of Multiplier circuit using conventional approach

The multiplier circuit shown in the above figure provide a single output which is Y (=$A_1.A_0$).

F. OR Circuit

The OR circuit performs the logical OR operation on the applied bits of the input signal. The conventional approach and block diagram of logical OR circuit is illustrated in figure 6.

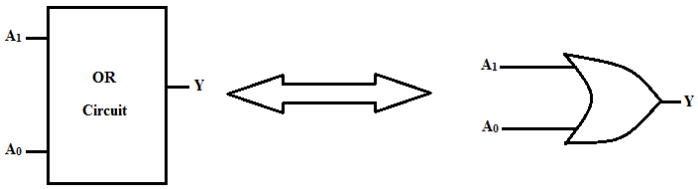


Fig 6: Block diagram and logic implementation of OR Circuit using conventional approach

Here output equation is $Y = A_1 + A_0$.

G. XOR Circuit

This part of the proposed ALU circuit performs the logical exclusive OR operation on the applied input bits. Figure 7 shows the block diagram and logical implementation of XOR circuit part of the proposed ALU circuit.

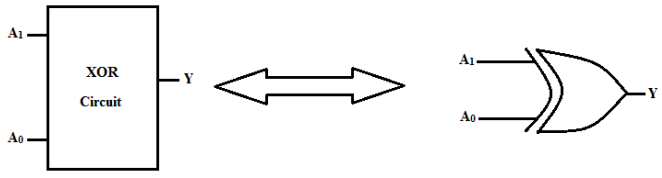


Fig 7: Block diagram and logic implementation of XOR Circuit using conventional approach

Output of XOR circuit is given as $Y = A_1 \oplus A_0$.

H. NAND Circuit

This circuit performs the logical NAND operation on the bits of the applied input signal. Figure 8 shows the block diagram as well as conventional design of this logical part of the target ALU circuit.

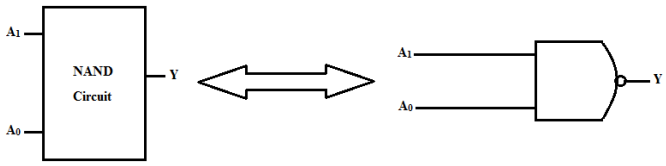


Fig 8: Block diagram and logic implementation of NAND Circuit using conventional approach

The output signal is shown in the following equation:
$Y = (A_1.A_0)'$;
Above operational sub-parts of the proposed Arithmetic Logic Unit circuit are multiplexed using 8:1 multiplexer for appropriate integration. Figure 9 provides the block diagram of proposed designed Arithmetic Logic Unit.

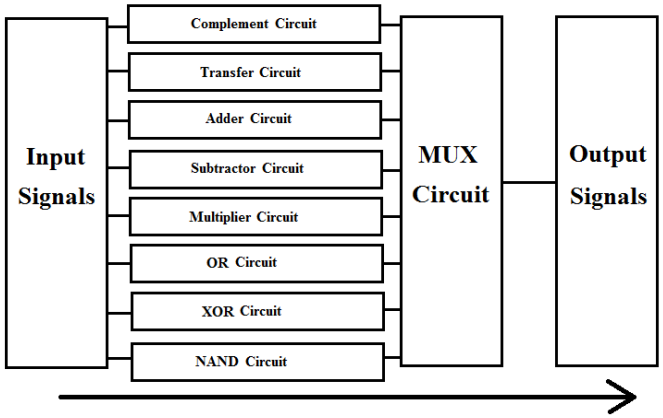


Fig 9: Block diagram of 2-bit Arithmetic Logic Unit Circuit

This ALU performs some arithmetic (addition, subtraction, multiplication etc) as well as some logical (OR, XOR, NAND etc) operations on the applied 2-bit binary signals. Function table for this ALU circuit is demonstrated in table 2 below.

TABLE II
FUNCTION TABLE OF 2-BIT BINARY ALU

S.No.	Selection Lines			Function Performed
	S_2	S_1	S_0	
1	0	0	0	2's Complement
2	0	0	1	Transfer Operation
3	0	1	0	Addition Operation
4	0	1	1	Subtraction Operation
5	1	0	0	Multiplication Operation
6	1	0	1	OR Operation
7	1	1	0	XOR Operation
8	1	1	1	NAND Operation

IV. PROPOSED 2-BIT ALU CIRCUIT USING REVERSIBLE LOGIC

Arithmetic Logic Unit (ALU) circuit shown in figure 9 is designed using conventional irreversible gates such as AND, OR, XOR gates etc. These gates generate information loss which further enhances the amount of heat generation from the circuit. So here we propose the design of the same 2-bit ALU circuit using reversible logic concept by changing the design entities with reversible logic gates. Following subsections provide the description of the design of required sub-circuits of the target ALU.

A. *Reversible Complement Circuit*

In figure 10 the reversible 2's complement circuit is designed using one Feynman gate for 2-bit binary number [12].

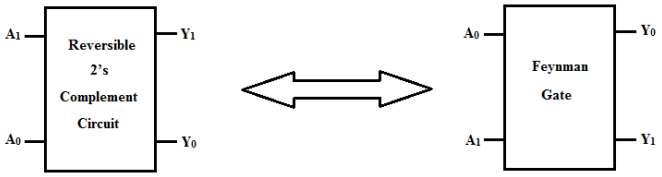


Fig 10: Block diagram and logic implementation of Reversible Complement Circuit

B. *Reversible Transfer Circuit*

Here only one Toffoli gate is required to transfer the applied 2- bit binary number to the output as illustrated in the figure 11 [16].

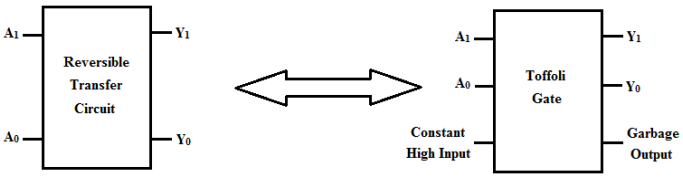


Fig 11: Block diagram and logic implementation of Reversible Transfer Circuit

C. *Reversible Adder Circuit*

This sub-part of the 2-bit ALU circuit is designed with the help of single Peres gate as shown in figure 12 [14].

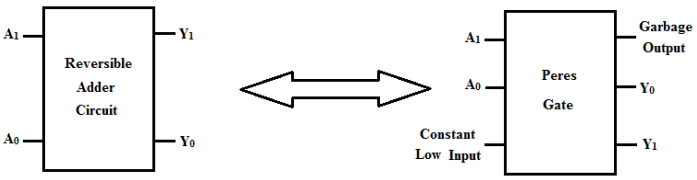


Fig 12: Block diagram and logic implementation of Reversible Adder Circuit

D. *Reversible Subtractor Circuit*

This reversible part of the aimed ALU circuit is designed using a single TR gate as shown in the figure 13 [15].

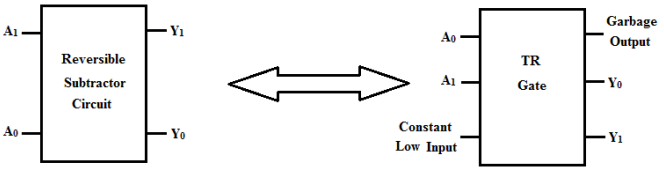


Fig 13: Block diagram and logic implementation of Reversible Subtractor Circuit

E. Reversible Multiplier Circuit

The two bit binary multiplier circuit with reversible logic concept is designed using single Toffoli gate as shown in figure 14 [16].

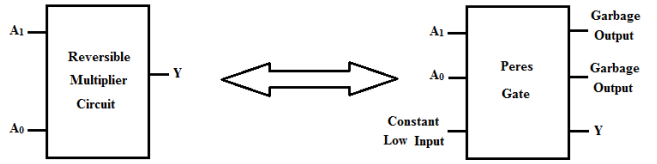


Fig 14: Block diagram and logic implementation of Reversible Multiplier Circuit

F. Reversible OR Circuit

The logical OR operation using reversible logic on the applied bits are implemented with the use of a single reversible logic URG gate as shown in figure 15 [10].

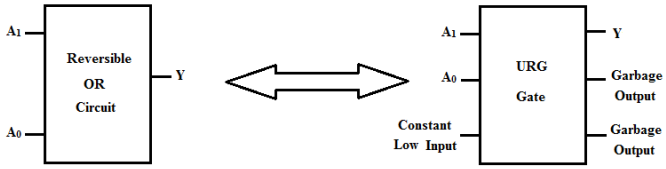


Fig 15: Block diagram and logic implementation of Reversible OR Circuit

G. Reversible XOR Circuit

This logical exclusive OR circuit using reversible logic is designed with the help of a single Feynman gate as shown in figure 16 [12].

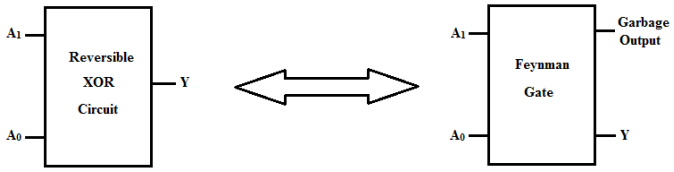


Fig 16: Block diagram and logic implementation of Reversible XOR Circuit

H. Reversible NAND Circuit

This part of the proposed ALU to perform logical NAND operation on the bits of the applied input signal with reversible logic concept is implemented using a single Peres gate as shown in figure 17 [14].

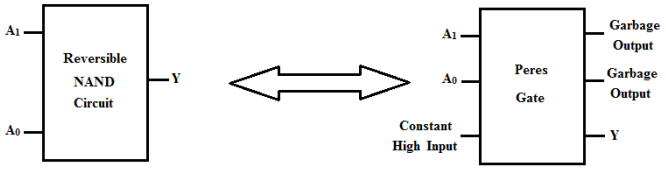


Fig 17: Block diagram and logic implementation of Reversible NAND Circuit

The 2-bit binary ALU circuits are designed through various reversible logic gates and integrated using 8:1 multiplexer. This optimized 8:1 multiplexer circuit uses two VSMT gate and one TKS gate as shown in the figure 18 [1,13,17].

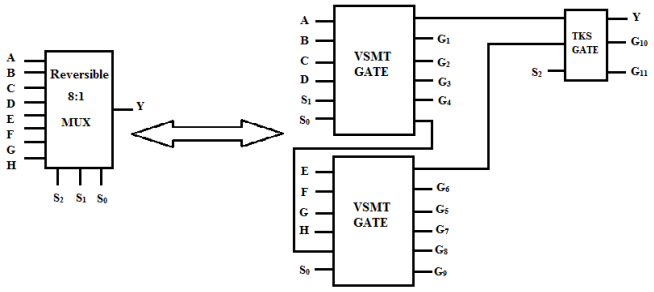


Fig 18: Block diagram of optimized 8:1 multiplexer circuit using reversible logic

Here G_1 to G_{11} are garbage output signals generated from the reversible circuit.

Proposed 2-bit Binary ALU Using Reversible Logic

The previous circuits are used in the designing of ALU by integration connections shown in figure 19.

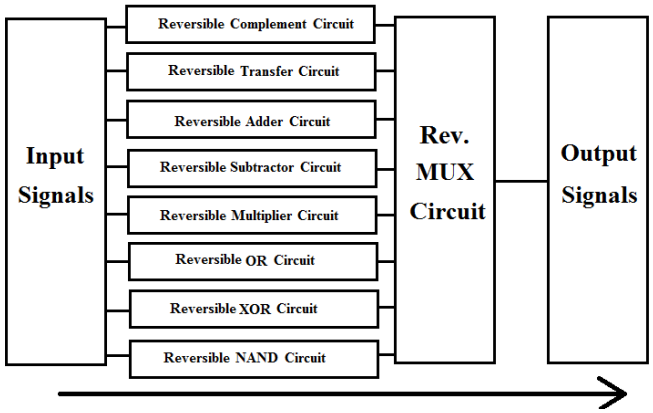


Fig 19: Block diagram of proposed 2-bit binary ALU circuit using reversible logic

The proposed ALU circuit using reversible logic conforms to the function table shown in table 2.

V. Result and Analysis

The proposed two bit arithmetic logic unit is simulated on Modelsim tool and synthesised for Xilinx Spartan 3E with Device XC3S500E with 200 MHz frequency. The simulation result of the proposed reversible logic based circuits are shown in figure 20.

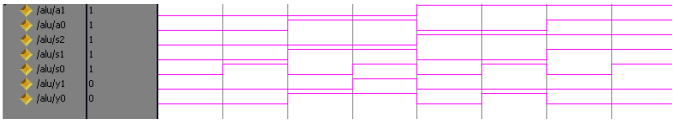


Fig 20: Simulated waveform of proposed 2-bit binary ALU circuits using Reversible Logic

In figure 20 the output of the proposed reversible circuit follows table 2. The synthesized circuit for proposed ALU using reversible gate is shown in Figure 21.

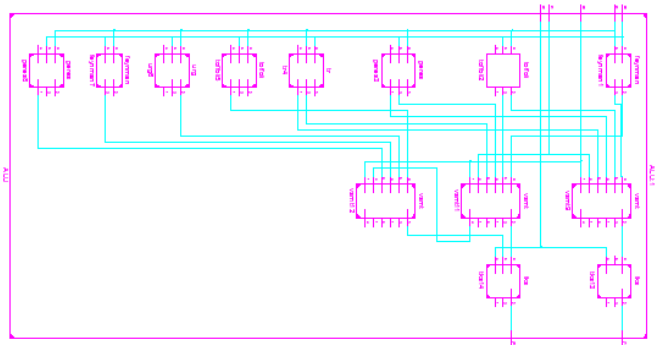


Fig 21: Synthesized circuit of proposed 2-bit binary ALU circuit using Reversible Logic

VI. Conclusion and Future Scope

We have proposed a novel design of 2-bit binary Arithmetic Logic Unit (ALU) circuit using reversible logic. The proposed ALU can perform some arithmetical and some logical operations utilizing the optimized 8:1 multiplexer circuit using reversible logic. The proposed ALU circuit can be further explored and employed to design and implement various other low power loss applications and help the researchers to design better devices/systems.

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